REMARKS/ARGUMENTS

Applicant would like to thank the Examiner for the careful consideration given the present application. The application has been carefully reviewed in light of the Office Action, and the following remarks are presented for the Examiner's consideration.

Claims 1-6 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,253,272 to Jaeger et al. (hereinafter "Jaeger"). For the following reasons, the rejection is respectfully traversed.

Regarding amended claims 1 and 5, Jaeger does not teach "a distributing unit that obtains an input digital signal and outputs the input digital signal to a plurality of devices respectively," as required. As claimed, the input digital signal is the *same* as the digital signal that is outputted from the distributing unit to the plurality of devices. Also, the *same* digital signal is outputted to each of the plurality of devices. To the contrary, Jaeger teaches a differential encoder and phase shifter (34) that outputs *two signals*: ADATA and BDATA. The two signals are *different* in that the phase of BDATA is shifted by one quarter of a cycle as compared to ADATA (see column 3, lines 43-49). Further, in Jaeger, the input signal inputted to the differential encoder and phase shifter (34) is different from the two output signals.

Further, regarding amended claims 1 and 5, Jaeger does not teach "a plurality of devices . . . . wherein *each* of the devices includes: . . . . a digital/analog converting unit that converts the digital signal regulated by the delay regulating unit to an analog signal; and an amplifying unit that amplifies the analog signal to output the amplified analog signal to the synthesizing unit." As claimed, each of a plurality of devices must include each of the listed components. First, Jaeger does not teach a plurality of digital/analog converting units. The Examiner indicates that since Jaeger describes a digital system, it must include "a DAC that converts the digital data into analog." Assuming, for purposes of argument, that Jaeger does include a digital-to-analog converter as the Examiner proposes, there is no reason why Jaeger would necessarily have a plurality of converters, i.e. one for each signal. Second, Jaeger clearly teaches a *single* amplifier (amplifier DC restoration circuit 74), not the plurality of amplifiers required by claims 1 and 5.

Thus, for at least the above reasons, Jaeger does not teach every limitation of the claims. Further, since claims 2-4 depend from claim 1, they are not anticipated for the same reasons. Therefore, claims 1-5 are not anticipated by Jaeger and the rejection should be withdrawn.

Regarding claim 6, Jaeger does not teach "a delay measuring method for a power combining system including a plurality of devices," as required. The Examiner does not indicate where the claimed method or any of the required steps are taught by the reference. Applicant respectfully submits that claim 6 is not anticipated by Jaeger and that the rejection should be withdrawn.

In consideration of the foregoing analysis, it is respectfully submitted that the present application is in a condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in a condition for allowance, the examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present application.

If there are any fees resulting from this communication, please charge same to our Deposit Account No. 16-0820, our Order No. NGB-41083.

Respectfully submitted,
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